University of Mumbai

Examination 2020

Program: BE Biomedical Engineering
Curriculum Scheme: Rev2012
Examination: Fourth Year Semester VII

Course Code: **BMC704 and** Course Name: **Very Large Scale Integrated Circuits**
Time: 1-hour Max. Marks: 50

==========

==========

Note to the students: - All the Questions are compulsory and carry equal marks.

Q1.	signal y:std_logic_vector(3 downto 0); what could be an assignment for y
Option A:	y<="0101"
Option B:	y<="01"
Option C:	y:="01"
Option D:	y:="0101"
Q2.	What is symbol used for high impedance state in VHDL
Option A:	Z
Option B:	X
Option C:	Y
Option D:	O
Q3.	State the statement which is compulsory in behavioral modeling.
Option A:	Process
Option B:	If
Option C:	While
Option D:	When
Q4.	Identify the invalid pair from the following.
Option A:	Structural modeling- Component statement
Option B:	Behavioral modeling- component statement
Option C:	Counter- clock signal
Option D:	Behavioral modeling- process statement
Q5.	In what aspect, HDLs differ from other computer programming languages?
Option A:	No aspect; both are same
Option B:	HDLs describe hardware rather than executing a program on a computer
Option C:	HDLs describe software and not hardware
Option D:	Other computer programming languages have more complexity
Q6.	which of the following statement will not come in any style of VHDL Code for 3 line to 8 line decoder
Option A:	Process statement
Option B:	when statement
Option C:	if clock' event and clock='1' then
Option D:	If Statement

Q7.	Variable declaration is done in architecture
Option A:	Before declaring architecture
Option B:	After begin process
Option C:	Before begin process
Option D:	Before begin architecture
Q8.	VHDL code for sequential counter cannot be done using
Option A:	Dataflow model
Option B:	Behavioral model
Option C:	Mixed model
Option D:	Sequential model
Q9.	In constant voltage scaling which entity remains constant?
Option A:	Gate capacitance
Option B:	Drain current
Option C:	Power dissipation
Option D:	Threshold voltage
Q10.	Surface mobility depends on
Option A:	effective drain voltage
Option B:	effective gate voltage
Option C:	channel length
Option D:	effective source voltage
Q11.	The current through enhancement type nMOSFET will flow when:
Option A:	$V_{gs} > V_{th}$, $V_{ds} = 0$
Option B:	$V_{gs} < Vth$, $V_{ds} > 0$
Option C:	$V_{gs} > V_{th}$, $V_{ds} > 0$
Option D:	$V_{gs} = 0$, $V_{ds} > 0$
Q12.	In Depletion load MOS inverter the pull up device is
Option A:	Depletion nMOS
Option B:	Resistor
Option C:	Enhancement nMOS
Option D:	pMOS
Q13.	In passive load inverter load device is
Option A:	nMOS
Option B:	Resistor
Option C:	pMOS
Option D:	Depletion nMOS
Q14.	Which statement is valid from the following statements?
Option A:	Threshold voltage for depletion type nMOSFET is positive.
Option B:	Threshold voltage for depletion type nMOSFET is negative.
Option C:	Threshold voltage for depletion type nMOSFET is zero.
Option D:	Threshold voltage concept is not applicable to depletion type MOSFET.

Q15.	In CMOS inverter when input and output are equal, driver and load transistor work in which modes?
Option A:	Driver- cut-off, Load- linear
Option B:	Driver- saturation, Load- linear
Option C:	Driver- saturation, Load- saturation
Option D:	Driver- linear, Load- cut-off
Q16.	When input voltage is $V_{IL,}$ what is the operating region of load transistor in depletion load nMOS inverter?
Option A:	Cut off region
Option B:	Saturation region
Option C:	Linear region
Option D:	Pinch off saturation
Q17.	Identify the wrong colour code from the given options
Option A:	n+ diffusion – green
Option B:	Buried contact – Brown
Option C:	implant – Yellow
Option D:	Contact cut – Blue
Q18.	In CMOS fabrication, wet etching is done using
Option A:	plasma
Option B:	hydrofluoric acid
Option C:	sulphuric acid
Option D:	sodium chloride
Q19.	Name the lithographic process which produces maximum resolution.
Option A:	X ray lithography
Option B:	Photolithography
Option C:	Electron beam lithography
Option D:	LASER lithography
Q20.	Identify the method not used for crystal growth?
Option A:	CZ method
Option B:	Bridgeman's method
Option C:	CVD method
Option D:	Float zone method
Q21.	Two metal layers can be joined by using
Option A:	contact cut
Option B:	Wire
Option C:	Via
Option D:	Glass
Q22.	On which layer Interconnection patterns are made?
Option A:	polysilicon layer
Option B:	silicon-di-oxide layer

Option C:	metal layer
Option D:	diffusion layer
Q23.	Which of the following effect is due to scaling?
Option A:	Short channel effect
Option B:	Channel length modulation
Option C:	Substrate bias effect
Option D:	Latch up effect
Q24.	Which statement is invalid?
Option A:	Silicon has larger band gap energy than Germanium
Option B:	Silicon has lower leakage current than Germanium
Option C:	Germanium is a cheaper material.
Option D:	Intrinsic resistivity of silicon is higher than Germanium.
Q25.	In the inverter design, which configuration produces least power dissipation?
Option A:	load as depletion nMOSFET
Option B:	load as enhancement nMOSFET
Option C:	load as pMOSFET(CMOS inverter)
Option D:	BiCMOS