Question Bank for S.E. (Sem-IV) Examination (A.Y. 2019-2020)

Code of Institute:	TSEC (238)
Branch:	COMPUTER
Sem:	IV
Subject Name (with Subject Code):	COA (CSC***)
Module Number and Title (if any):	Entire syllabus
Number of questions:	**10**

Important Note: All Questions Compulsory.
        Only one option is correct for each question.
        Each question carries 0.5 mark each.

Q. No.		
1		**Which of the following is NOT true about Control and Status registers**
	(a)	Not visible to the programmer.
	(b)	They are used by control unit.
	(c)	These are accessible to the programmer.
	(d)	These are privileged registers and used by operating system programs only.
2		**Which of the following is NOT true about condition codes**
	(a)	Condition codes are the bits that are set as a result of some ALU operation
	(b)	They are called as Flags
	(c)	Programmer can explicitly refer and alter them
	(d)	They are transparent to the programmer
3		**Consider a memory module of 1024 locations. Each location can store 16 bits of information. What is the size of the memory, size of address bus, size of data bus and size of decoder?**
	(a)	Size: Memory- 1024X 16 B, address bus = 10bits, data bus=4 bits, decoder: 10:1024
	(b)	Size: Memory- 1024X 16 bits, address bus = 1024 bits, data bus=16 bits, decoder: 1024:10
	(c)	Size: Memory- 16KB, address bus = 10bits, data bus=16 bits, decoder: 10:1024
	(d)	Size: Memory- 1024B, address bus = 10 bits, data bus=4 bits, decoder: 1024:10
4		**More opcodes in fixed length Instruction Format means**
	(a)	More bits in opcode field and less bits for addressing
	(b)	More bits for the instruction length, more bits in the opcode field and less bits for addressing
	(c)	More bits in instruction length, more bits in the opcode field and more bits in the addressing
	(d)	More bits in the instruction length, less bits in the opcode field
5		**Variable length instruction can provide the following variations**
	(a)	Large no of opcodes, Different opcode lengths and Flexible addressing
	(b)	Large no of opcodes and Flexible addressing

	(c)	Small number of opcodes but different opcode lengths
	(d)	Large number of opcodes with Fixed opcode lengths
6		**Identify the addressing mode in the following instruction: Add (R1), R2**
	(a)	Indirect addressing
	(b)	Direct addressing
	(c)	Register Indirect
	(d)	Register Addressing
7		**Which of the following instruction cycle states involve indirection?**
	(a)	Operand Fetch, operand store and operand address calculation
	(b)	Operand Fetch, operand store
	(c)	Operand fetch, operand address calculation
	(d)	Operands store, operand address calculation
8		**For Interrupts choose Incorrect option**
	(a)	The processor can be engaged in executing other instructions while an I/O operation is in progress.
	(b)	The processor's efficiency cannot be improved
	(c)	IO modules can interrupt the normal processing of the processor
	(d)	ISR is executed by the processor in response to an interrupt
9		**Where does the interrupt breakpoint occur?**
	(a)	After the Fetch Cycle is completed
	(b)	Before Instruction address Calculation
	(c)	Before Fetch Cycle
	(d)	After Operand Store is completed
10		**Which of the following is an example of Software Interrupt?**
	(a)	Division by zero
	(b)	Power Failure
	(c)	Service request from Printer
	(d)	Service request from Keyboard

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