

Digital System Design

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Electronics and Telecommunication

Sem-3 (ECC0330)

1	Any signed negative binary number is recognised by its _____
	a)MSb
	b)LSB
	c)Byte
	d)Nibble
	Answer – (a)
2	The decimal equivalent of the binary number $(1011.011)_2$ is _____
	a) $(11.375)_{10}$
	b) $(10.123)_{10}$
	c) $(11.175)_{10}$
	d) $(9.23)_{10}$
	Answer –(a)
3.	The quantity of double word is _____
	a) 16 bits
	b) 32 bits
	c) 4 bits
	d) 8 bits
	Answer –(b)
4.	Perform binary addition: $101101 + 011011 = ?$
	a) 011010
	b) 1010100
	c) 101110
	d) 1001000
	Answer – (D)
5.	What is the minimum number of two input NAND gates used to perform the

	function of two input OR gates?
	a)One
	b)Two
	c)Three
	d) Four
	Answer-(c)
6.	The following switching functions are to be implemented using a decoder: $f_1 = \sum m(1, 2, 4, 8, 10, 14)$ $f_2 = \sum m(2, 5, 9, 11)$ $f_3 = \sum m(2, 4, 5, 6, 7)$ The minimum configuration of decoder will be _____
	a) 2 to 4 line
	b) 3 to 8 line c) 4 to 16 line
	c) 4 to 16 line
	d) 5 to 32 line
	Answer – (c)
7.	The full form of DIP is _____
	a) Dual-in-Long Package
	b) Dual-in-Line Package
	c) Double Integrated Package
	d) Double-in-Line Package
	Answer – (d)
8.	Propagation delay is defined as _____
	a) the time taken for the output of a gate to change after the inputs have changed
	b) the time taken for the input of a gate to change after the outputs have changed
	c) the time taken for the input of a gate to change after the intermediates have changed
	d) the time taken for the output of a gate to change after the intermediates have changed
	Answer –(a)
9.	How many NAND circuits are contained in a 7400 NAND IC?
	a)1

	b)2
	c)4
	d)8
	Answer – (c)
10.	Each “1” entry in a K-map square represents:
	a) A HIGH for each input truth table condition that produces a HIGH output
	b) A HIGH output on the truth table for all LOW input combinations
	c) A LOW output for all possible HIGH input conditions
	d) A DON’T CARE condition for all possible input truth table combinations
	Answer –(a)
11.	Which of the following statements accurately represents the two BEST methods of logic circuit simplification?
	a) Actual circuit trial and error evaluation and waveform analysis
	b) Karnaugh mapping and circuit waveform analysis
	c) Boolean algebra and Karnaugh mapping
	d) Boolean algebra and actual circuit trial and error evaluation
	Answer – (c)
12.	Which is the major functioning responsibility of the multiplexing combinational circuit?
	a) Decoding the binary information
	b) Generation of all minterms in an output function with OR-gate
	c) Generation of selected path between multiple sources and a single destination
	d) Encoding of binary information
	Answer—(c)
13	Most demultiplexers facilitate which type of conversion?
	a) Decimal-to-hexadecimal
	b) Single input, multiple outputs
	c) AC to DC
	d) Odd parity to even parity

	Answer—(b)
14.	How is an encoder different from a decoder?
	a) The output of an encoder is a binary code for 1-of-N input
	b) The output of a decoder is a binary code for 1-of-N input
	c) The output of an encoder is a binary code for N-of-1 output
	d) The output of a decoder is a binary code for N-of-1 output
	Answer-(a)
15.	If two inputs are active on a priority encoder, which will be coded on the output?
	a) The higher value
	b) The lower value
	c) Neither of the input
	d) Both of the inputs
	Answer—(a)
16	The primary use for Gray code is _____
	a) Coded representation of a shaft's mechanical position
	b) Turning on/off software switches
	c) To represent the correct ASCII code to indicate the angular position of a shaft on rotating machinery
	d) To convert the angular position of a shaft on rotating machinery into hexadecimal code
	Answer –(a)
17.	Which of the following is correct for a gated D-type flip-flop?
	a) The output complement follows the input when enabled
	b) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
	c) Only one of the inputs can be HIGH at a time
	d) The output toggles if one of the inputs is held HIGH
	Answer—(b)
18.	In JK flip flop same input, i.e. at a particular time or during a clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock

	pulse the value of output Q is uncertain. The situation is referred to as?
	a) Conversion condition
	b) Race around condition
	c) Lock out state
	d) Forbidden State
	Answer—(b)
19.	To realise one flip-flop using another flip-flop along with a combinational circuit, known as _____
	a) PREVIOUS state decoder
	b) NEXT state decoder
	c) MIDDLE state decoder
	d) PRESENT state decoder
	Answer—(b)
20.	The only difference between a combinational circuit and a flip-flop is that _____
	a) The flip-flop requires previous state
	b) The flip-flop requires next state
	c) The flip-flop requires a clock pulse
	d) The flip-flop depends on the past as well as present states
	Answer—(c)
21.	FPGA stands for _____
	a) Full Programmable Gate Array
	b) Full Programmable Genuine Array
	c) First Programmable Gate Array
	d) Field Programmable Gate Array
	Answer—(d)
22.	Volatile memory refers to _____
	a) The memory whose loosed data is achieved again when power to the memory circuit is removed
	b) The memory which loses data when power to the memory circuit is removed

	c) The memory which loses data when power to the memory circuit is applied
	d) The memory whose lost data is achieved again when power to the memory circuit is applied
	Answer—(b)
23.	On subtracting $(001100)_2$ from $(101001)_2$ using 2's complement, we get _____
	a) 1101100
	b) 011101
	c) 11010101
	d) 11010111
	Answer—(b)
24.	Add the two BCD numbers: $1001 + 0100 = ?$
	a) 10101111
	b) 01010000
	c) 00010011
	d) 00101011
	Answer—(c)
25.	What does minuend and subtrahend denotes in a subtractor?
	a) Their corresponding bits of input
	b) Its outputs
	c) Its inputs
	d) Borrow bits
	Answer—(c)