

Program: BE –EXTC

Curriculum Scheme: Choice based R-16

Examination: Second Year Semester III

Course Code: and Course Name: EDC I

SAMPLE QUESTION PAPER

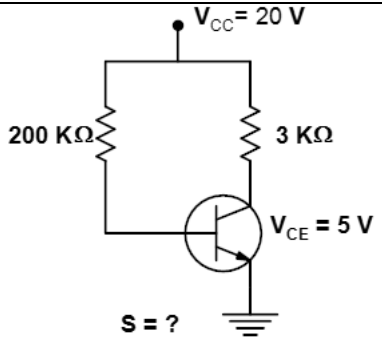
Time: 1 hour

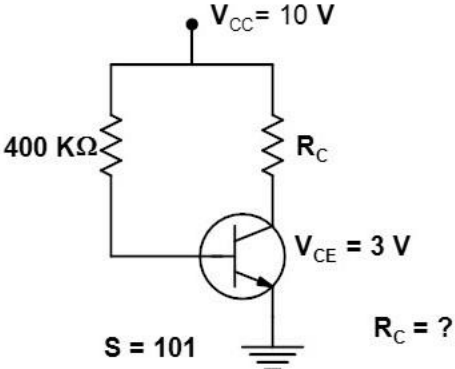
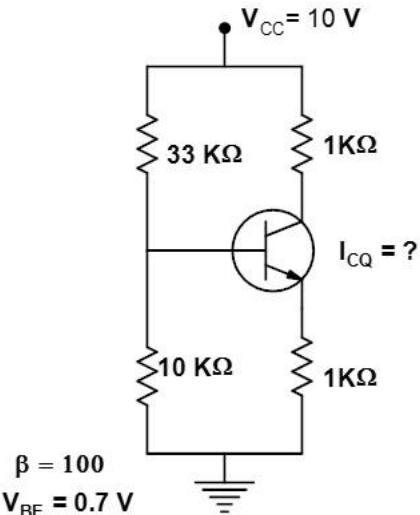
Max. Marks: 50

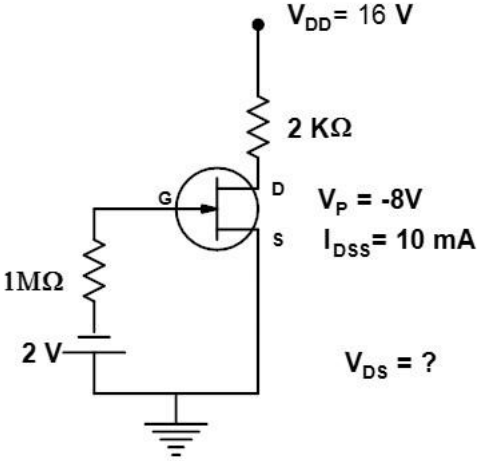
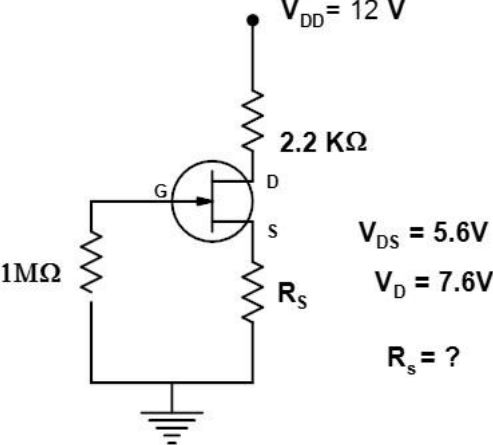
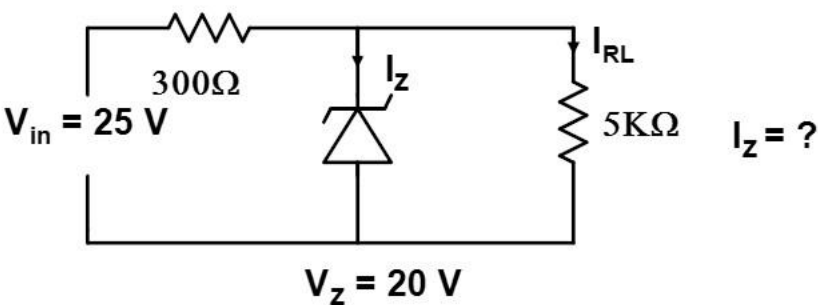
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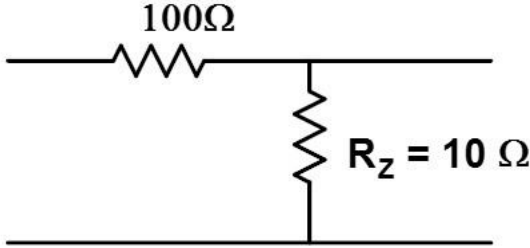
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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	If for a transistor $\beta = 100, I_{CBO} = 10\mu A, I_B = 50\mu A$ then $I_E =$
Option A:	10 mA
Option B:	6.06 mA
Option C:	6.06A
Option D:	10A
Q2.	For a transistor $\alpha = 0.99, I_{CBO} = 5\mu A$ and $I_E = 8.5$ mA then $I_B =$
Option A:	$80\mu A$
Option B:	$75\mu A$
Option C:	$100\mu A$
Option D:	$50\mu A$
Q3.	
Option A:	100.813
Option B:	80.813
Option C:	52.813
Option D:	50.813

Q4.	 <p>$V_{CC} = 10 \text{ V}$</p> <p>$400 \text{ K}\Omega$</p> <p>R_C</p> <p>$V_{CE} = 3 \text{ V}$</p> <p>$S = 101$</p> <p>$R_C = ?$</p>
Option A:	2K Ω
Option B:	5K Ω
Option C:	2.2K Ω
Option D:	3K Ω
Q5.	 <p>$V_{CC} = 10 \text{ V}$</p> <p>33 KΩ</p> <p>1KΩ</p> <p>$I_{CQ} = ?$</p> <p>10 KΩ</p> <p>1KΩ</p> <p>$\beta = 100$</p> <p>$V_{BE} = 0.7 \text{ V}$</p>
Option A:	1.61 mA
Option B:	2 mA
Option C:	3.13 mA
Option D:	2.61 mA
Q6.	For a p-channel FET $V_p = 5\text{V}$ $I_{DSS} = 10\text{mA}$ and $V_{GS} = 1\text{V}$
Option A:	1mA
Option B:	6.4mA
Option C:	5mA
Option D:	1.5 mA

Q7.	 <p> $V_{DD} = 16\text{ V}$ $2\text{ K}\Omega$ $V_P = -8\text{ V}$ $I_{DSS} = 10\text{ mA}$ $V_{DS} = ?$ </p>
Option A:	8V
Option B:	4.75V
Option C:	5V
Option D:	6V
Q8.	 <p> $V_{DD} = 12\text{ V}$ $2.2\text{ K}\Omega$ $V_{DS} = 5.6\text{ V}$ $V_D = 7.6\text{ V}$ $R_S = ?$ </p>
Option A:	1KΩ
Option B:	2Ω
Option C:	5KΩ
Option D:	3KΩ
Q9.	 <p> $V_{in} = 25\text{ V}$ 300Ω I_Z $5\text{ K}\Omega$ I_{RL} $V_Z = 20\text{ V}$ $I_Z = ?$ </p>
Option A:	10 mA
Option B:	12.67 mA
Option C:	10.57 mA
Option D:	4mA

Q10.	During fabrication process of passive elements to permit selective etching ,the SiO ₂ layer must be subjected to a
Option A:	Oxidation process
Option B:	Epitaxial Growth process
Option C:	Metalization Process
Option D:	Photolithographic Process
Q11.	Average DC voltage of a full wave rectifier circuit is given as
Option A:	$2V_M/\pi$
Option B:	V_M/π
Option C:	$V_M/2\pi$
Option D:	$V_M/2$
Q12.	Consider the simplified diagram of a Zener shunt regulator .The dynamic impedance of zener is 10Ω.Find the voltage stability factor.
	
Option A:	0.091
Option B:	10
Option C:	11
Option D:	1
Q13.	For an n-channel JFET V _p = -2V the value of V _{GS} for zero current drift will be
Option A:	-2.63V
Option B:	-1.37V
Option C:	+1.37V
Option D:	+2.63V
Q14.	In hybrid pi model of transistor, value of g _m and r _π is given by
Option A:	ICQ/VT and βVT/ICQ respectively
Option B:	βVT/ICQ and ICQ/VT
Option C:	ICQ, and βVT
Option D:	None of above
Q15.	While drawing AC equivalent circuit of any amplifier
Option A:	VCC retained and capacitors replaced by short circuit
Option B:	VCC connected to gnd, capacitors replaced by short circuit
Option C:	Capacitors are retained and Vcc connected to gnd
Option D:	None of the above

Q16.	In any two port network if feedback impedance is Z After using Millers theorem Z1 and Z2 are as follows
Option A:	$Z1=Z/1-k$, and $Z2=Zk/K-1$
Option B:	$Z1=Z/K-1$, and $Z2=Z/K-1$
Option C:	$Z1=ZK/K-1$ and $Z2=Z/k-1$
Option D:	None of the above
Q17.	Bipolar junction transistor operates in
Option A:	Can not work as an amplifier and as a switch
Option B:	Saturation as amplifier and active region and cutoff region as a switch
Option C:	Active region as amplifier and cannot be used as a switch
Option D:	Active region for amplifier and in cut off and saturation as a switch
Q18.	h parameters of bjt can be found from input, output characteristics
Option A:	hie and hre from input characteristics and hfe and hoe from output characteristics
Option B:	hfe ,hoe from input characteristics and hie and hre from input characteristics
Option C:	hfe ,hre from input characteristics and hie and hoe from input characteristics
Option D:	hre ,hoe from input characteristics and hie and hfe from input characteristics
Q19.	Current flowing into the gate terminal when it is biased in saturation region is
Option A:	Highest
Option B:	Zero
Option C:	lowest
Option D:	None of the above
Q20.	Voltage gain formula for common drain amplifier or source follower is
Option A:	$gmRs/1+gmRs$
Option B:	$gmRs$
Option C:	1
Option D:	None of the above
Q21.	Factors affecting the bandwidth of RC coupled amplifier
Option A:	Coupling and bypass capacitors and interelectrode capacitors
Option B:	Capacitors do not decide the bandwidth
Option C:	Low frequency and high frequency cut off depends on resistor values
Option D:	None of the above
Q22.	Function of bypass capacitor in CE amplifier is
Option A:	To provide high reactance path for amplified signal appearing at emitter.
Option B:	To provide low reactance path to amplified signal at emitter

Option C:	Output obtained at collector does not change with or without CE
Option D:	CE does not play any vital role in CE amplifier
Q23.	Shockley Equation for JFET is
Option A:	$ID=IDSS[1-VGS/VP]^2$
Option B:	$ID=Vp[1-VGS/Vp]$
Option C:	$Vp=ID[1-VGS/VP]$
Option D:	None of the above
Q24.	Equation for Zero temperature drift for JFET is
Option A:	$ VP-VGS =0.63$
Option B:	$ VGS-VP =0.64$
Option C:	$ VP-VGS =1$
Option D:	None of the above
Q25.	Calculation of value of resistance RD if volage gain of common source amplifier Is given as $ Av =10, gm=1.26mS, rd=50k$
Option A:	6k
Option B:	5k
Option C:	9.424k
Option D:	3k