Examination: Second Year Semester IV

Course Code: ITC404

Course Name: Computer Organization and Architecture

Time: 1hour Max. Marks: 50

==========

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	What does CISC stand for?
Option A:	Circuit Instruction Set Computer
Option B:	Complex Instruction Set Computer
Option C:	Complex Instruction Set Circuit
Option D:	Compact Instruction Set Computer
Q2.	The major drawback of RISC processors are
Option A:	Poor code density, non-executable x86 code
Option B:	High code density, non-executable x86 code
Option C:	Poor code density, executable x86 code
Option D:	High code density, executable x86 code
Q3.	The number of Instructions in RISC is ____ as compared to CISC.
Option A:	Less
Option B:	More
Option C:	Complex
Option D:	Variable
Q4.	In Von-Nuemann architecture
Option A:	Data and instructions are stored in same memory
Option B:	Data and instructions are not stored in same memory
Option C:	Data is stored in memory
Option D:	Instructions are stored in memory
Q5.	RISC stands for
Option A:	Restricted Instruction Sequential Compiler
Option B:	Restricted Instruction Sequencing Computer
Option C:	Reduced Instruction Set Computer
Option D:	Reduced Integrated Sequential Compiler
Q6.	Which of the following is not an addressing mode?
Option A:	Direct addressing mode
Option B:	Register addressing mode

Option C:	Immediate addressing mode
Option D:	Arithmetic addressing mode
Q7.	If the decimal point is placed to the right of the first significant digit, then the number is called _____
Option A:	Orthogonal
Option B:	Normalized
Option C:	Determinate
Option D:	Decimal
Q8.	In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.
Option A:	16
Option B:	20
Option C:	23
Option D:	24
Q9.	The 32 bit representation of the decimal number is called as _____
Option A:	Decimal Number
Option B:	Single Precision
Option C:	Double Precision
Option D:	Extended Format
Q10.	In double precision format, the size of the mantissa is _____
Option A:	32 bits
Option B:	64 bits
Option C:	128 bits
Option D:	256 bits
Q11.	Why characteristic makes RAM unsuitable for permananet Storage?
Option A:	Volatile
Option B:	Speed
Option C:	Size
Option D:	Reliability
Q12.	The memory implemented using the semiconductor chips is _____
Option A:	Cache
Option B:	Main
Option C:	Secondary
Option D:	Registers
Q13.	Which of the following is used for binary multiplication?
Option A:	Restoring Algorithm
Option B:	Booth's Algorithm
Option C:	Pascal's Rule

Option D:	Digit by Digit multiplication
Q14.	What is the default value of accumulator in booth's multiplication of two 4-bit binary numbers?
Option A:	0
Option B:	1
Option C:	0000
Option D:	00000
Q15.	What is the value of n in multiplication of 110* 1000?
Option A:	0
Option B:	2
Option C:	3
Option D:	4
Q16.	The number of sign bits in a 32-bit IEEE format is _____
Option A:	1
Option B:	9
Option C:	11
Option D:	23
Q17.	What is the high speed memory between the main memory and the CPU called?
Option A:	Register memory
Option B:	Cache memory
Option C:	Storage memory
Option D:	Virtual Memory
Q18.	Whenever the data is found in the cache memory it is called as _____
Option A:	HIT
Option B:	MISS
Option C:	FOUND
Option D:	ERROR
Q19.	The reason for the implementation of the cache memory is _____
Option A:	To increase the internal memory of the system
Option B:	The difference in speeds of operation of the processor and memory
Option C:	To reduce the memory access and cycle time
Option D:	To reduce Power Dissipation
Q20.	The effectiveness of the cache memory is based on the property of _____
Option A:	Locality of reference
Option B:	Memory Localisation
Option C:	Memory Size

Option D:	Volatility
Q21.	The algorithm to remove and place new contents into the cache is called _____
Option A:	Replacement Algorithm
Option B:	Renewal Algorithm
Option C:	Updation Algorithm
Option D:	Erasing Algorithm
Q22.	The chip by which both the operation of read and write is performed _____
Option A:	RAM
Option B:	ROM
Option C:	PROM
Option D:	EPROM
Q23.	RAM is also known as _____
Option A:	RWM
Option B:	MBR
Option C:	MAR
Option D:	ROM
Q24.	If a RAM chip has n address input lines then it can access memory locations upto _____
Option A:	$2^{(n-1)}$
Option B:	$2^{(n)}$
Option C:	$2^{(n+1)}$
Option D:	$2^{(2n)}$
Q25.	Which one of the following is volatile in nature?
Option A:	ROM
Option B:	EPROM
Option C:	PROM
Option D:	RAM