# Thadomal Shahani Engineering College University of Mumbai Sample Paper KT Examination December 2020 <br> Program: Information Technology Engineering Curriculum Scheme: Rev2016 <br> Examination: Second Year Semester III Course Code: ITC302 and Course Name: Logic Design 

For the students:- All the Questions are compulsory and carry equal marks .

| Q1. | To work as an Amplifier, transistor should operate in which region? |
| :---: | :---: |
| Option A: | Saturation region |
| Option B: | Cut-off region |
| Option C: | Active region |
| Option D: | Inverse-Active region |
| Q2. | A transistor has a $\beta_{D C}$ of 200 and a base current, $I_{B}$, of $8 \mu \mathrm{~A}$. The collector current, $\mathrm{I}_{\mathrm{c}}$, equals: |
| Option A: | 180 A |
| Option B: | 16.5 mA |
| Option C: | 180 mA |
| Option D: | 1.6 mA |
| Q3. | Which of the following set represents the coordinates of Q point? |
| Option A: | (Vc, Ic) |
| Option B: | ( $\mathrm{V}_{\mathrm{CE}, \mathrm{Ic}}$ ) |
| Option C: | $\left(\mathrm{V}_{\mathrm{BE}}, \mathrm{I}_{\mathrm{B}}\right)$ |
| Option D: | (Vcc, Ic) |
|  |  |
| Q4. | Which of the factor in transistor does not get affect due to change in temperature? |
| Option A: | $\mathrm{I}_{\text {CE }}$ |
| Option B: | $\beta$ |
| Option C: | $\mathrm{V}_{\text {BE }}$ |
| Option D: | $\mathrm{R}_{\mathrm{B}}$ |
| Q5. | Nibble consists of how many bits? |
| Option A: | 4 |
| Option B: | 8 |
| Option C: | 12 |
| Option D: | 16 |
| Q6. | Conversion of (869) ${ }_{10}$ to (1000 0110 1001) represent conversion from Decimal to which code? |
| Option A: | Binary |
| Option B: | Gray |
| Option C: | BCD |

## Thadomal Shahani Engineering College

## University of Mumbai

Sample Paper KT Examination December 2020

| Option D: | Hexadecimal |
| :---: | :--- |
|  |  |
| Q7. | A binary code can be converted to excess-3 using which of the following gates |
| Option A: | AND |
| Option B: | OR |
| Option C: | NOT |
| Option D: | XOR |
|  |  |
| Q8. | What will the binary value for octal number (377 ) 8 |
| Option A: | 11111111 |
| Option B: | 101010111 |
| Option C: | 11011111 |
| Option D: | 111111000 |
|  |  |
| Q9. | Which of the following is not a valid law in Boolean algebra |
| Option A: | Exponential Law |
| Option B: | De morgans law |
| Option C: | Absorption law |
| Option D: | Commutative law |
|  |  |
| Q10. | Which of the following expression is in SOP form |
| Option A: | (ABC) (B'C'A) (A'B) |
| Option B: | (A+B) (A'+B'+C') |
| Option C: | ABC + B'C'A + A'B |
| Option D: | AB'(A'+C) |
|  |  |
| Q11. | Which of the following is universal gate |
| Option A: | OR |
| Option B: | XOR |
| Option C: | NOR |
| Option D: | NOT |
|  |  |
| Q12. | XOR gate , could be represented using which of the following expressions |
| Option A: | A xor B = A'B' |
| Option B: | A xor B =AB' + A'B |
| Option C: | A xor B = AB + A'B' |
| Option D: | A xor B = B'(AB)A' |
|  |  |
| Q13. | Which of the following are correct equation for half adder |
| Option A: | Sum = A+B, Carry = AB |
| Option B: | Sum = A xor B , Carry = AB |
| Option C: | Sum = A'B', Carry = A'B |
| Option D: | Sum = AB, Carry = A+B' |
| Synchronous circuits |  |

## Thadomal Shahani Engineering College

## University of Mumbai

Sample Paper KT Examination December 2020

| Option B: | Encoder circuit |
| :---: | :---: |
| Option C: | Decoder circuit |
| Option D: | Binary Adder Circuit |
| Q15. | An encoder have the following combination of Input and Output. |
| Option A: | n Inputs, $2^{\text {n }}$ Outputs |
| Option B: | n Inputs, n Outputs |
| Option C: | $2^{\mathrm{n}}$ Inputs, n Outputs |
| Option D: | 1 input, n Outputs |
| Q16. | In the given 4-to- 1 multiplexer, if $\mathrm{c} 1=0$ and $\mathrm{c} 0=1$, what will be the value of M |
| Option A: | $\mathrm{X}_{3}$ |
| Option B: | $\mathrm{X}_{2}$ |
| Option C: | $\mathrm{X}_{1}$ |
| Option D: | $\mathrm{X}_{0}$ |
| Q17. | DeMultiplexer can implement the logic of which of the following |
| Option A: | OR gate |
| Option B: | Multiplexer |
| Option C: | Encoder |
| Option D: | Decoder |
| Q18. | In a J-K flip-flop, if $\mathrm{J}=\mathrm{K}$ the resulting flip-flop is referred to as |
| Option A: | D flip-flop |
| Option B: | SR flip flop |
| Option C: | D flip flop |
| Option D: | T flip flop |
| Q19. | The flip flop is cativated by |
| Option A: | Negative edge trigger |
| Option B: | Positive edge trigger |
| Option C: | Either Positive or Negative edge trigger |
| Option D: | Sinusoidal trigger |
| Q20. | For a counter, if all flip-flops receive same clock signal. Then such counter is called as |
| Option A: | Up Counter |
| Option B: | Down Counter |

## Thadomal Shahani Engineering College <br> University of Mumbai

Sample Paper KT Examination December 2020

| Option C: | Asynchronous Counter |
| :---: | :--- |
| Option D: | Synchronous counter |
|  |  |
| Q21. | A register is |
| Option A: | a memory location used for caching information |
| Option B: | a group of flip-flops used for storing 1 bit information |
| Option C: | a group of flip-flops used for storing $n$ bits binary information |
| Option D: | a group of flip-flops used for storing text message |
|  |  |
| Q22. | Ripple counter is also known as |
| Option A: | Decade Counter |
| Option B: | Ring Counter |
| Option C: | Synchronous counter |
| Option D: | Asynchronous counter |
|  |  |
| Q23. | In VHDL, which of the following is a valid name for an entity |
| Option A: | And_gate |
| Option B: | OR gate |
| Option C: | NAND |
| Option D: | NOR |
|  |  |
| Q24. | Which of the following is correct command to perform XNOR operation in VHDL |
| Option A: | U <= !(A xor B); |
| Option B: | U <= A exnor B; |
| Option C: | U <= A xnor B; |
| Option D: | U <= A ^xor B; |
|  |  |
| Q25. | A package in VHDL consists of |
| Option A: | Commonly used functions, procedures |
| Option B: | Commonly used architectures |
| Option C: | Commonly used tools |
| Option D: | Commonly used syntax and variables |

