Q.1 In 8086 microprocessor, the address bus is _____ bit wide.

A. 12 bit

B. 10 bit

C. 16 bit

D. 20 bit

Q.2 The memory management of 80386 supports

A. virtual memory

B. paging

C. four level of protection

D. all of these

Q.3 In 8257 (DMA), each of the four channels has

A) a pair of two 8-bit registers

B) a pair of two 16-bit registers

C) one 16-bit register

D) one 8-bit register

Q.4 Port C of 8255 can function independently as

A) input port

B) output port

C) either input or output ports

D) both input and output ports

Q.5 During the instruction cycle of 80386, any debug fault can be ignored if

A. VM flag is set

B. RF flag is set

C. RF flag is cleared

D. VM flag is cleared

Q.6 In a cascaded mode, the number of vectored interrupts provided by 8259A is

A) 4

B) 8

C) 16

D) 64

Answers

Q.7 The Floating point registers of IA-32 can operate on operands up to _____

A) 128 bit

B) 256 bit

C) 80 bit

D) 64 bit

Q.8. After every response to the single step interrupt the flag that is cleared is

A) IF (Interrupt Flag)

B) TF (Trap Flag)

C) OF (Overflow Flag)

D) None of the mentioned

Q.9 The instruction that pushes the contents of the specified register/memory location on to the stack is

a) PUSHF

b) POPF

c) PUSH

d) POP

Q.10 In which T-state does the CPU sends the address t o memory or I/O and the ALE signal

for demultiplexing

(A) T1.

(B) T2.

(C) T3.

(D)T4.